REMARKS

Claims 1-8 are currently pending in the application. No amendment is made to the claims or to the drawings. No new matter is added.

Claims 1-8 are rejected under *35* U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the Examiner objects that claim 1 is read on different embodiments and specifically that “Figure 2 and figure 5 are two completely different embodiments. The "a continuous-time sigma-delta modulator", 8, in figure 2 cannot be a part of the circuit of figure 5 and the "a delay means" cannot be a part of the circuit of figure 2.”

It is submitted that page 3 lines 16-22 of the specification clearly states: “Figure 2 is a block schematic diagram of a continuous-time Digital-to-Analogue sigma-delta modulator to which the present invention may be applied” and “Figure 5 is a block schematic diagram of a clock pulse generator”. Page 7 lines 9-11 states: “Unlike the prior art techniques, this embodiment of the present invention avoids interfering with the normal operation of the circuit” (of Figure 1 or 2) “ but rather focuses on attenuating jitter within the clock signal before it is applied to the circuit.” Page 7 lines 26-28 states: “This is achieved with a clock generator using a local time reference built using a delay line 14 and a logic AND/NAND circuit 15, as shown in Figure 5.”. It is submitted that the specification clearly describes that the invention utilizes the clock generator of Figure 5 to generate the clock signals for the continuous-time sigma-delta modulator of Figure 1 or 2 and that claim 1 is directed to the combination of the continuous-time sigma-delta modulator with the clock pulse generator recited. See also originally filed claim 6 where it states “wherein said continuous-time sigma-delta means comprises a digital-to-analogue converter means (5; 9) whose operation is responsive to said train of combined clock pulses (CLK_JF).” Thus, circuit 5 in Figure 1 and circuit 9 in Figure 2 are responsive to the clock pulses (CLK_JF) (see Figures 5 and 8).”

The Examiner objects that “the AND/NAND circuit is not seen in any Figure.” However, the sentence bridging pages 7-8 of the specification clearly states “Both the

clock and the delayed clock (CLK_D) signals are applied as inputs to the logic AND/NAND circuit 15", which is shown as a logic block in Figure 5.

The Examiner states: "Assume that the combiner is circuit (15, OR gate) in figure 9, This OR gate cannot perform the function shown the timing diagram of figure 5." Applicant submits that the specification does not identify the OR gate of Figure 8 or 9 with the timing diagram of Figure 6, the embodiment of clock generator shown in Figure 8 being another embodiment of 'a combiner for producing a train of combined clock pulses presenting leading and trailing edges defined alternately by one of said delayed edges and the corresponding edge of the primary clock pulse' as defined in claim 1, in which the OR gate performs the function of 'combiner' of claim 1 in conjunction with the two inverters at its two inputs.

The Examiner objects that: "The recitation "the variability of said widths of said active clock phases being smaller than the variability of the positions of said leading and trailing edges" on lines 15 - 17 is confusing". The examiner's attention is respectfully directed to the fact that the clause does not (and cannot) read as the Examiner suggests: 'said widths of said active clock phases being smaller' but reads "the variability ... being smaller'. Indeed, the active clock phases vary less in width than do the non-active clock phases, in accordance with the present invention.

Regarding claim 2, the Examiner states "the recitation "first series of delay elements" is confusing because it is not clear what it is in the drawing. Assume that this "said first series of delay elements" is element (16) in figure 9 then this recitation lacks antecedent basis." Applicant submits that "said first series of delay elements" has antecedent in 'at least a first series of delay elements" recited in lines 2-3 of claim 2, and refers to series 14 of substantially identical elements 16 shown in Figures 7, 8 & 9, for example.

Regarding claim 3, it is submitted that "a further series of cascaded delay elements" in lines 2-3 of claim 3 clearly provides an antecedent for "said further series of cascaded delay elements" in lines 6 and 8. "said train of primary clock pulses" has a clear antecedent in "a train of return-to zero primary clock pulses" in claim 1 at line 6 (as amended). The adjustment element corresponds to phase detector 25 and LPF 26 of Figure 9, which respond to the delay of the 'further series' 23 to tend to correct that

delay by applying the adjustment signal Vtune, which is then applied also to adjust the delay defined by the first series 14.

Regarding claim 5, the specification states at page 8 lines 20-22 “In a typical application to a sigma delta module, the active phase ACP is preferably used as the phase where the integration is performed while the NACP is used for returning to zero”. Indeed, the integrators 2 of Figure 1 integrate the signal from the DAC 5 which samples the signal Y from the output over periods defined by the widths of the active clock phases (ACP) as specified in claim 5.

Regarding claims 6 to 8, Applicant submits that “said train of combined clock pulses” has antecedent in claim 1 line 12. The clock signal CLK_JF of Figure 5 is clearly stated in the specification to be the clock signal utilized in Figure 1 or 2, which show the clock signal applied to the ADC 4 and DACs 5 and 9.

Accordingly, it is submitted that claims 1 to 8 are allowable. Issue of a patent on this application is requested.

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action since reasons for the patentability of each pending claim are provided without addressing these statements. Therefore, Applicants reserve the right to address these statements at a later time if necessary.

No amendment made herein is related to the statutory requirements of patentability unless expressly stated herein. Further, no amendment herein is made for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

SEND CORRESPONDENCE TO:

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